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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,831	ZAMMIT ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-13 have been presented for examination. Claims 1-13 have been rejected.

Priority

1. The Examiner acknowledges Applicants' request for priority to Great Britain application 0030735.5 filed on December 15, 2000. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Technology Background

To better facilitate a discussion of the prior art, the Examiner provides the following technology background.

"Operating System Concepts, Sixth Edition" by Silbershatz, Galvin, and Gagne (Silbershatz), ©2002, contributes to establishing what was well known in the prior art. Most relevant to Applicants' claimed invention are the teachings regarding *process scheduling* (sections 4.2-4.2.3). Silbershatz teaches a *job queue* and a *ready queue* (page 99). Processes wait in the ready queue until they are *dispatched* to a CPU (page 100). A process can be taken off the CPU for several reasons, ultimately returning to the ready queue to be dispatched once again, until the process terminates (page 100; Figure 4.5). The task of switching the CPU to another process is known as a *context switch* (page 103).

Silbershatz also teaches *preemptive scheduling* (pages 153-154). Silbershatz also teaches preemption as a method of recovering from deadlock (page 265).

Additional teachings by Silbershatz may be relevant to establishing what was well known in the prior art.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 10-12 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims recite method steps that decide a problem known in computer science as the Halting Problem, which is proven to be unsolvable. The Examiner respectfully draws Applicants' attention to "Introduction to the Theory of Computation", by Michael Sipser, ©1997, particularly section 5.1.

3. To summarize the teachings of Sipser, it is impossible to determine *a priori* whether a set of instructions will halt. The only way to correctly determine this in the general case is to simulate the operation of the instructions to see if the simulation halts. However, if the set of instructions is an infinite loop, the simulation will similarly execute an infinite loop. At any given point in time during the potentially infinite loop, it is

impossible to know, without error and in the general case, whether the instructions indeed form an infinite loop or whether the loop will eventually terminate. The Halting Problem is extremely well known in computer science and can be found in almost any computation textbook.

4. The Examiner appreciates that Applicant has not explicitly recited a solution to the Halting Problem. The Examiner respectfully presumes that Applicant did not intend to claim such an invention. However, the specification (page 49, line 14 – page 51, line 2) describes this method in a way that would include solving the Halting Problem (particularly page 50, lines 13-14) and claims 10-12 are similarly broad. As a result, the method of the claimed invention includes a method of solving the Halting Problem, which has been shown as impossible, and a person of ordinary skill in the art could not make and use the claimed invention.

5. The Examiner respectfully suggests amended claim language that clarifies what is meant by "analyzing the loop termination condition" and what is meant by "possible non-terminating". The Examiner readily admits that the disclosed method would be enabled under certain circumstances and for certain interpretations of the terms cited above and therefore recommends claim language that is limited to those circumstances and interpretations.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-19 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites limitations including "at least one first programming language" (preamble, lines 2-3), "at least one high-level hardware description language" (step (a), lines 9-10), and "the at least one first language" (step (b), lines 14-15). It is unclear whether "the at least one first language" in step (b) refers to the "at least one first programming language" of the preamble or the "at least one high-level hardware description language" of step (a).

8. Claim 1 recites a concluding step of "applying the at least one software model in the at least one first language and the at least one second model in the at least one second language to the simulation engine" however it is unclear what is meant by "applying to the simulation engine". It is unclear whether this should be interpreted as a step of initializing the simulation engine or a step of performing the simulation.

9. Claims 10-12 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims recite limitations regarding determining whether a loop condition is "possibly non-terminating" which has several distinct interpretations. The most concrete interpretation is a loop which is executed at least once is "possibly non-terminating", meaning that only `while(0)` or an equivalent which is never entered, is a definitely terminating loop. A second interpretation is a loop that may or may not terminate depending on the processing of data values that can only

be determined by simulating the loop. This interpretation is the subject of the Halting Problem as discussed above. A third interpretation is a `for` loop wherein the loop variable is manipulated within the body of the loop. It is possible, but not provable, that such a loop will be non-terminating, although this is a broad, blanket statement based on a superficial analysis of the loop.

10. Claim 16 recites the limitation "an apparatus" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 16 should be an independent claim for an apparatus rather than depending from claim 1 that recites a method. As amended, claim 16 should incorporate all of the necessary limitations from claim 1 that define the claimed invention. Claim 17 should similarly dependent from an amended independent claim 16.

11. Claim 18 recites the limitation "a computer program" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 18 should be an independent claim for a computer program rather than dependent from claim 17 that recites an apparatus. As amended, claim 18 should incorporate all of the necessary limitations from claim 1 that define the claimed invention.

12. Claim 19 recites "a storage medium containing a program" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 19 should be an independent claim for a storage medium, or dependent upon an amended independent claim 16 for an apparatus, rather than dependent upon claim 18 that recites a computer program. As amended, claim 19 should incorporate all of the necessary limitations from claim 1 that define the claimed invention.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependency.

Claim Interpretation

In the interest of compact prosecution, the Examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

13. Claim 1 has been interpreted where "the at least one first language" in step (b) refers to "at least one first programming language" of the preamble. Claim 1 has been interpreted where "applying to the simulation engine" means "providing as input and performing the simulation".

14. Claims 10-12 cannot be interpreted without relying on speculation. The Examiner presumes the intended bounds of these claims lie somewhere between the Halting Problem and a superficial analysis of the loop as described above, however cannot determine precisely where that bound should lie with any confidence. The Examiner presumes that the purpose of these steps is to recover from a deadlock scenario among concurrent processes by interrupting loop execution, thereby implementing a type of preemptive scheduling among the concurrent processes. The Examiner has interpreted these claims in an attempt to remain true to the spirit of the invention and apologizes if these interpretations are inappropriate.

15. Claim 13 appears to recite additional steps of the method of claim 1 that are performed by a human operator. The steps of "checking whether the result of the co-

simulation is correct" and "checking whether the digital circuit is synthesisable" appear to be steps of human cognition. It is therefore not unreasonable to interpret the step of "generating a low-level hardware description of the digital circuit" as performed by a human, perhaps by using a computer aided design system of prior art. This reasonable interpretation of claim 13 results in limitations that are entirely performed by a human being. If Applicant feels this interpretation is improper, clarification is respectfully requested.

16. Claims 16-19 have been interpreted as suggested above in the section regarding rejections under 35 U.S.C. § 112, second paragraph. Claim 16 is regarded as independent. Claim 17 is regarded as depending from claim 16. Claim 18 is regarded as independent. Claim 19 is regarded as independent.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

17. Claims 1-19 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

18. Regarding claim 1, MPEP 2106 (II) (A) reads as follows:

> The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." *State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02*. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (*Brenner v. Manson*, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); *In re Ziegler*, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain

> some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful.

Claim 1 recites "a method of co-simulating" which does not produce a useful, concrete, and tangible result. The recited steps include "providing at least one first model", "converting the at least one first model", "providing at least one second model", and concludes with "applying the at least one software model in the at least one first language and the at least one second model in the at least one second language to the simulation engine". As indicated above, the proper interpretation of the concluding step of claim 1 is unknown, however it appears that no reasonable interpretation would produce a useful, concrete, and tangible result as required by MPEP 2106 (II) (A).

19. The Examiner respectfully suggests claim language that clearly sets forth the useful, concrete, and tangible result, such as a simulation output that is displayed to a user or otherwise transmitted outside the computer.

20. Regarding claims 18 and 19, MPEP 2106 reads as follows:

> Similarly, computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. Accordingly, it is important to distinguish claims that define descriptive material per se from claims that define statutory inventions.

Claim 18 recites a computer program *per se* and is therefore directed to nonstatutory subject matter. Claim 19 recites "a storage medium containing a program as claimed in claim 18", however this recitation is not limited to a *computer-readable medium* and is

therefore not directed to the technological arts. A paper printout of the computer program of claim 18 would teach the limitations of claim 19 however would be nonstatutory subject matter.

Claims not specifically mentioned stand rejected by virtue of their dependence.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claims 1- are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,870,588 to Rompaey et al. (Rompaey).

23. Regarding claim 1, Rompaey teaches a method of simulating a digital system comprising simultaneous low-level and high-level simulation (column 6, lines 35-44). Rompaey calls the design environment for this simulation "CoWare" (column 10, lines 53-62). CoWare supports high-level hardware description language models of system

components (column 11, lines 45-58; DFL, VHDL) as well as hardware description language models (column 12, lines 45-50). Naturally the high-level programming language models need to be compiled before they can be simulated (column 17, lines 29-58). The CoWare system supports four major design activities, including co-simulation (column 11, lines 12-15). The claimed invention is disclosed with an exemplary embodiment (summarized at column 22, lines 26-35).

24. Therefore Rompaey anticipates the invention of claim 1 by teaching a co-simulation system where a first portion of the system can be modeled in a high-level programming language as a first model, the first model is converted by compiling the high-level programming language, a second portion of the system can be modeled in a second language, and the overall system is co-simulated by executing both the first model and the second model and simulating their interaction.

25. Regarding claim 2, Rompaey teaches the converting step comprises compiling the first model (column 12, lines 45-50).

26. Regarding claim 3, Rompaey teaches that the high-level hardware language is based on a communicating sequential process model (column 11, line 59 – column 12, line 5).

27. Regarding claim 4, Rompaey teaches that the first part of a digital system is represented as a plurality of concurrent processes that communicate with each other

(column 11, line 59 – column 12, line 5; column 12, lines 23-34) and converting the concurrent processes to a sequential software process (column 12, lines 44-49; column 16, lines 6-17; column 16, lines 24-30).

28. Regarding claim 5, Rompaey teaches a port and protocol hierarchy that distinguishes between the functional and communication behavior (column 16, line 31-65). Included in this are references to a *handshake* (column 16, lines 42-45). A handshake is functionally equivalent to a stimulus and a response.

29. Regarding claim 6, Rompaey teaches a port and protocol hierarchy that distinguishes between the functional and communication behavior (column 16, line 31-65). It is inherent that components in CoWare respond to the stimulus by performing a desired behavior of at least one part of the digital system. This concept is the premise of Rompaey's invention; violating this premise would render the invention useless.

30. Regarding claim 7, Rompaey teaches an exemplary embodiment including a sample clock generator (column 21, lines 34-59). As CoWare is a computer-implemented system (column 15, lines 50-62) and, in at least one embodiment, executes concurrent processes on a single processor (column 22, lines 52-59), it is inherent that CoWare uses a scheduler. Failure to use a scheduler, as well known in the art, would diminish the utility of the system such that it would be nearly inoperable.

31. Regarding claim 13, Rompaey teaches steps of synthesizing the circuit (column 11, lines 12-20) and generating a low-level hardware description of the circuit (column 28, lines 23-30).

32. Regarding claim 14, Rompaey teaches that the disclosed system is to be used as a method of manufacturing a circuit (column 6, lines 7-18).

33. Regarding claims 16-19, Rompaey teaches that the disclosed system is embodied on a computer apparatus (column 15, lines 50-62). The CoWare system interfaces with an application programmer's interface (API) (column 15, lines 50-52) therefore it is inherent that the CoWare system is a computer program. It is inherent that the computer program is stored on a computer-readable medium.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 8-12 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rompaey.

36. Claims 8, 9, 11, and 12 recite limitations regarding a scheduler. Official notice is taken that all of the recited capabilities or functions of the scheduler are well known in

the art. While it is inherent that the system of Rompaey uses some form of scheduler, the particular features of that scheduler may not be inherent. However, it would have been obvious to a person of ordinary skill in the art to incorporate well-known capabilities and functions of a scheduler with the scheduler of Rompaey in order to benefit from the well-known properties of those capabilities and features.

37. Claims 10-12 recite limitations regarding modification of a program loop to implement a type of preemptive scheduling. Official notice is taken that preemptive scheduling is well known in the art. It would have been obvious to implement preemptive scheduling with the scheduler of Rompaey when designing a system with concurrent processes in order to avoid deadlock scenarios, a well-known advantage of preemptive scheduling.

38. Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Rompaey in view of "Pentium® Pro Processor Performance Brief" by Intel, © 1997.

39. Regarding claim 15, Intel shows a well-known integrated circuit (entire document, especially pages 5-6). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to produce an integrated circuit, such as the Pentium® Pro Processor, using the method disclosed by Rompaey.

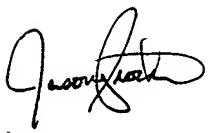
Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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